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DRAWINGS ATTACHED

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(54) FIELD EFFECT TRANSISTORS FOR INTEGRATED CIRCUITS AND METHODS OF MANUFACTURE

(71) We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organized according to the laws of the State of Delaware, United States of America, of 13500 North Central 5 Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described 10 in and by the following statement:—

This invention relates to integrated circuit devices including *p*-channel field effect transistors and processes for fabricating such circuits. —

15 It is frequently desired to fabricate differential/operational amplifiers which have high gain, a low noise figure, high output voltage swing and balanced amplifier stages. These requirements can be attained 20 when good quality *n*-channel and *p*-channel field effect transistors as well as NPN and PNP bipolar transistors are included on a single integrated circuit bar. However, prior 25 differential/operational amplifier integrated circuits have not included complementary field effect transistors, have low input impedances, and less than satisfactory output stage characteristics. There are numerous other design situations that cannot be satisfactorily met by known techniques but could be advantageously resolved by providing 30 complementary *n*- and *p*-channel field effect transistors of high quality and performance.

It is an object of this invention to provide 35 a method of fabricating an integrated circuit including a field effect transistor having a channel of *p*-type conductivity.

According to one aspect of the invention there is provided a method of fabricating a 40 semiconductor integrated circuit comprising forming a plurality of isolated semiconductor devices in a monolithic chip including forming a *p* type channel field effect transistor by epitaxially growing an *n*-type layer 45 of semiconductor material of over an *n*-type

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region diffused in one surface of a semiconductor substrate, forming a *p*-type channel region partially through the epitaxially grown layer above said *n*-type region; diffusing isolation rings through the epitaxial layer 50 about each of the electrical components including the field effect transistor; further diffusing downwardly the channel region and upwardly the *n*-type region diffused in the semiconductor substrate to form a *p-n* junction in the epitaxial layer between said regions, and forming *p*-type source and drain regions, and an *n*-type gate region in said channel region. —

According to a second aspect of the invention there is provided a semiconductor integrated circuit comprising a plurality of isolated semiconductor devices including a *p* type channel field effect transistor formed in a monolithic chip, said field effect transistor having a *p*-type region formed in a semiconductor substrate, a diffused *n*-type back gate region formed in said *p*-type region, an *n*-type epitaxial layer grown over said back gate region, a *p*-type channel 65 region diffused partially through the epitaxial layer above said back gate region, said channel region extending downwardly and said back gate region extending upwardly to form a *p-n* junction therebetween in said 70 epitaxial layer, isolation rings formed about each of the semiconductor devices including the field effect transistor, and *p*-type source and drain regions and an *n*-type front gate region formed in said channel region. —

In the accompanying drawings, in which various possible embodiments of the invention are illustrated:—

Figure 1 is a schematic or representational cross-section of a substrate illustrating *p*-type diffused regions of different circuit devices formed in the first of several successive steps of the embodiment in which the several devices are concurrently fabricated; —

Figure 2 shows the regionally diffused 90

substrate of Figure 1 including further diffused $n+$ subepitaxial regions formed in a subsequent process step;

Figure 3 illustrates the substrate of Figure 5 2 following the formation of an epitaxial layer;

Figure 4 shows the substrate of Figure 3 after a second p -type diffusion step;

Figure 5 illustrates the substrate of Figure 10 4 after a third p -type diffusion to form isolation rings and after the p -type region of Figure 4 is further diffused or driven further into the epitaxial layer while the opposing $n+$ region is advanced to form a junction 15 therewith;

Figure 6 shows the substrate of Figure 5 after a fourth p -type diffusion;

Figure 7 illustrates the substrate of Figure 20 6 following a second n -type diffusion; and Figure 8 is a schematic or representational cross-section of a substrate illustrating another embodiment of this invention.

Corresponding reference characters indicate corresponding parts throughout the 25 several views of the drawings.

Referring now to Figures 1-7 of the drawings, the starting material for a first method of fabricating the devices or integrated circuits of this invention is a slice or substrate 30 10 sawed from single crystal silicon 3-5° off of 1-1-1 orientation and lightly doped with a suitable n -type dopant, such as phosphorus, and having a typical resistivity of approximately 10-20 ohm-cm. It is mechanically polished to a mirror smooth finish and thermally oxidized at a temperature of, 35 typically, 1200°C. Throughout the following description conventional techniques of photoresist operations, masking, etching and acid clean-up steps are utilized, all as well known to those skilled in this art, and in order to avoid obscuring the important process steps and structural aspects of this invention these conventional techniques will 40 45 not be described or illustrated.

The first diffusion step is carried out to form p -type conductivity regions 12a-d (Figure 1) into one face of substrate 10 in the areas or zones NC, PC, NPN and PNP 50 55 defined by appropriate diffusion windows (not illustrated) in a conventional masking layer. A p -type impurity, such as boron, is employed in this conventional diffusion step (e.g., boron tribromide at 850°C. for about one hour followed by heating in an oxygen atmosphere at 1250°C. for about 40 hours) simultaneously to form these first p -type regions 12a-d in substrate 10, each having a depth of about 100 lines and a surface concentration of approximately 10^{16} atoms/cm³. Region 12a will provide a back gate for an n -channel FET (field effect transistor) while regions 12b, 12c and 12d will provide electrical isolation for a p -channel FET, an NPN 60 65 vertical bipolar transistor, and a PNP sur-

face bipolar transistor, respectively.

A first n -type diffusion is performed through appropriate windows (not shown) in zones PC, NPN and PNP to effect a relatively slow diffusion of an n -type diffusant (such as antimony or arsenic) by conventional diffusing techniques to form subepitaxial $n+$ regions 14b, 14c and 14d (Figure 2). These regions are relatively heavily doped, having a surface concentration of about 10^{19} atoms/cm³ and extend into p -type regions 12b-d about 50 lines. Region 14b forms a back gate for the p -channel FET being formed in zone PC. Region 14c forms a low resistivity subsurface path for current to the collector region of the NPN transistor being formed in zone or substrate portion NPN. Region 14d serves to prevent parasitic PNP action relative to substrate 10. The oxide layers resulting from this 85 diffusion are removed and the slice surface is cleaned and prepared for epitaxial layer growth.

A lightly doped n -type epitaxial layer 16 is then grown (Figure 3) to a depth of 90 0.35-0.40 mils by any suitable customary epitaxial process, such as thermally decomposing trichlorosilane in a hydrogen atmosphere containing a few parts per million of arsenic. The resistivity of epitaxial layer 16 95 is in the range 2-4 ohm-cm. A second p -type diffusion is then performed through a window (not shown) to extend partially through epitaxial layer 16 in zone PC (Figure 4) to form a lightly doped p -type 100 region 18b. Again this is done by conventional diffusion methods such as by a relatively low temperature (e.g. 850°C.) diffusion for about one hour using boron tribromide in nitrogen as the impurity source followed 105 by heating in a steam atmosphere at 1000°C. for another 1-2 hours. The depth of this p -type diffused region is about 8 lines and has a surface concentration of approximately 10^{16} atoms/cm³. This region will form the 110 channel region of the p -channel FET.

After removing narrow bands of the resulting oxide (on the upper face of layer 16) around the peripheries of zones NC, PC, NPN and PNP, a p -type dopant, e.g., boron, 115 is diffused into and through the epitaxial layer 16 to form heavily doped $p+$ barrier or isolation rings 20a-20d (Figure 5) which contact the peripheries of p -type regions 12a-12d respectively, and which have a surface concentration of about 10^{20} atoms/cm³. This diffusion is performed by heating the slice 10, for example, in an atmosphere of boron tribromide in nitrogen at a temperature of 1150°C. for about an hour followed 120 by further heating in an oxygen atmosphere at 1250°C. for about another 2 hours. Not only are the p -type barrier rings 20a-20d formed (which permits effective isolation of each of the devices from the n -type substrate 130

by reverse biasing), but this effects a further diffusion which drives the $n+$ regions 14b-d upwardly into the epitaxial layer as indicated by the dashed lines in Figure 5. Currently this further diffusion causes the lower or opposing surface of p -type region 18b to move downwardly about 7 lines to form a junction or interface with n -type region 14b. It is to be understood that this further diffusion may be performed independently instead of concurrently with the fourth diffusion forming the barrier or isolation rings. It will also be noted that the first p -type regions 12a-12d also are driven upwardly as indicated in Figure 5 by the dashed lines. As the epitaxial layer 16 is about 0.35 mils or about 30 lines in depth and the fronts of p -type regions 12a and 12b and the front of the $n+$ region 14b have moved or further diffused upwardly about 15 lines, this provides channel regions 22a and 22b in zones NC and PC of about 15 lines in depth. That is, the fronts of regions 12a, 12b and 14b at the interfaces between these regions and the undersurface of the epitaxial layer 16 move at substantially the same rate upwardly into layer 16 and at a rate somewhat more rapid than the downward advancing of the lower face of region 18b. Thus the depths (the distances between the top of epitaxial layer 16 and the advanced fronts of regions 12a, 12b and 14b) of channels 22a and 22b of both the n -channel and p -channel FETs being formed are substantially identical. Thus, this further diffusion step permits an advantageous close and convenient control of the depths of these channel regions and provides a marked improvement in the quality and characteristics of the n - and p -channel FETs fabricated in accordance with this invention.

A further p -type diffusion is performed (Figure 6) by conventional methods (e.g., boron tribromide at 975°C. for about $\frac{1}{2}$ hour followed by further heating at 1150°C. for about 1 hour) to convert the n -type epitaxial layer 16 in regions 24a, 24bs, 24bd, 24c, 24dc, 24de and R to p -type regions having a depth of about 8 lines and a typical surface concentration (boron) of about 5×10^{18} atoms/cm³. Region 24a of zone NC constitutes a diffused front gate of the n -channel FET being formed and is of strip form intersecting isolation ring 20a which is in turn electrically connected to the back gate region 12a. Regions 24bs and 24bd form the source and drain contacts of the p -channel FET being fabricated in zone PC. P -type region 24c forms the base of the NPN transistor in zone NPN, while region 24dc forms a ring shaped collector and region 24dc constitutes an emitter for PNP transistor in zone PNP. Region R forms a diffused surface resistor of a desired length.

65 An n -type impurity, such as phosphorus,

is employed in a second n -type, and final, diffusion to form relatively heavily doped (surface concentration of about 10^{21} atoms/cm³) $n+$ regions 26as, 26ad, 26b, 26ce, 26cc and 26d having a depth of about 6 lines. 70 Regions 26as and 26ad form source and drain contacts for the n -channel FET fabricated in zone NC, while 26b forms the diffused front gate region of the p -channel FET fabricated in zone PC. This region 26b 75 extends into the epitaxial layer 10 in zone PC and is therefore connected therethrough to the $n+$ back gate region 14b. $N+$ regions 26ce and 26cc respectively form the emitter and the collector contact of the NPN vertical 80 bipolar transistor fabricated in zone NPN. Region 26d constitutes the base contact for the surface bipolar PNP transistor formed in zone PNP.

The integrated circuit devices are completed by customary selective etching and applying metal where desired by conventional evaporation and photoresist-etch techniques thereby to form the ohmic connections and interconnections and the surface 85 metal leads desired.

Thus the above described exemplary process of the present invention not only fabricates p -channel FET devices, but can concurrently fabricate high quality n -channel FET devices, complementary NPN and PNP transistors, and resistors all on the same monolithic integrated circuit chip. It will be understood that subepitaxial resistors and other structures known to those 95 skilled in the integrated circuit art may be conveniently included without further substantial process steps. Also, it should be noted that if no n -channel FET is to be concurrently fabricated, a lightly doped p -type (instead of an n -type) silicon slice or substrate 10 is used for the starting material and the first p -type diffusion is omitted. The p -channel FET so fabricated effects virtually no degradation in the other devices 100 formed on the same integrated circuit slice and provides additional design flexibility 105 and improved circuit performance. For example, on all FET amplifier and other versatile designs optimizing performance beyond 110 previously attainable capabilities may be fabricated in accordance with this invention. Differential/operational amplifiers so fabricated have a high gain, a low noise figure, high output voltage swing and well-balanced 115 amplifier stages.

Figure 8 illustrates an alternative embodiment demonstrating the flexibility of the methods of the present invention. In this instance a lightly doped p -type silicon substrate or slice 10a is employed as a starting material rather than the n -type slice 10. As no n -channel FET is to be formed, the first diffusion to form the p -type diffused regions 12a-d is eliminated. In Figure 8 therefore 120 125 130

the portions of the *p*-type substrate underlying the zones where devices PC', NPN' and PNP' are formed constitute the first *p*-type regions of these devices. In all other respects the process steps for fabricating the integrated circuit of Figure 8 are the same as described above in regard to Figures 1-7, the first diffusion in this latter exemplary method being the *n*-type diffusion to form 10 *n*-type regions 14b'-14d'. The *p*-channel FET formed in zone PC', the vertical bipolar NPN transistor formed in zone NPN', and the surface bipolar PNP transistor formed in zone PNP' are virtually respectively identical 15 to those described in Figures 1-7, the reference numerals in Figure 8 being annotated with a prime designation to refer to regions which correspond to those already described above.

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WHAT WE CLAIM IS:—

1. A method of fabricating a semiconductor integrated circuit comprising forming a plurality of isolated semiconductor devices 25 in a monolithic chip including forming a *p*-type channel field effect transistor by epitaxially growing an *n* type layer of semiconductor material over an *n* type region diffused in one surface of a semiconductor 30 substrate, forming a *p*-type channel region partially through the epitaxially grown layer above said *n*-type region; diffusing isolation rings through the epitaxial layer about each of the electrical components including the 35 field effect transistor; further diffusing downwardly the channel region and upwardly the *n*-type region diffused in the semiconductor substrate to form a *p-n* junction in the epitaxial layer between said regions, and forming 40 *p*-type source and drain regions and an *n*-type gate region in said channel region.

2. A method according to Claim 1, wherein said *n*-type region is formed by diffusing *n*-type conductivity producing 45 material into a first *p*-type region in said one substrate surface.

3. A method according to Claim 2, wherein said first *p*-type region is formed by diffusing a *p*-type conductivity producing 50 material into said one surface of an *n*-type substrate.

4. A method according to Claim 2 or 3 wherein a vertical bipolar NPN transistor is also formed by diffusing during the first *n*-type diffusion and prior to growing the *n*-type epitaxial layer another *n*-type region 55 into another *p*-type region underlying the area where the *n-p-n* transistor is to be formed; and after growing the *n*-type epitaxial layer on the substrate diffusing a *p*-type base region partially through said *n*-type epitaxial layer during the diffusion of the *p*-type source and drain regions for the *p*-channel field effect transistor; and diffusing 60 a *n*-type emitter region partially through

the base region and a *n*-type collector contact region partially through the *n*-type epitaxial layer during the diffusion of the *n*-type gate region for the *p*-channel field effect transistor.

5. A method according to any of Claims 2 to 4, wherein a surface bipolar PNP transistor is also formed by diffusing during the first *n*-type diffusion and prior to growing the *n*-type epitaxial layer another *n*-type region 70 into another *p*-type region underlying the area where the *p-n-p* transistor is formed, and after growing the *n*-type epitaxial layer on the substrate diffusing *p*-type emitter and collector regions partially through the epitaxial layer during the diffusion of the *p*-type source and drain regions for the *p*-channel field effect transistor and a *n*-type base contact region partially through the epitaxial layer during the 80 diffusion of the *n*-type gate for the *p*-channel field effect transistor.

6. A method according to any preceding Claim wherein a *n*-channel field effect transistor is formed simultaneously with the *p*-channel field effect transistor by diffusing during the diffusions of the *p*-type source and drain regions for the *p*-channel field effect transistor a *p*-type gate region on an *n*-type region to form the channel of the 90 *n*-channel field effect transistor in the *n*-type epitaxial layer over a *p*-type region diffused in the substrate, and diffusing *n*-type source and drain contact regions for the channel of the *n*-channel field effect transistor during 95 the diffusion of the *n*-type gate region of the *p*-channel field effect transistor.

7. A method according to any of Claims 2 to 6 wherein the circuit components are 100 isolated by diffusing through the epitaxial layer into the first *p*-type regions *p*-type isolation rings which are more heavily doped than adjacent *p*-type regions.

8. A method according to Claim 7, wherein said *p*-type isolation rings are 110 formed during the further diffusion of said *p*-type channel region downwardly into the epitaxial layer and said *n*-type region upwardly into said epitaxial layer.

9. A method according to Claim 1, 115 wherein the *n*-type epitaxial layer is grown over a *n*-type region diffused into a substrate of *p*-type conductivity; the *p*-type channel region is formed by diffusing partially through the aforesaid epitaxial layer, the 120 isolation rings are diffused through the epitaxial layer to the *p*-type substrate while diffusing the *p*-type channel downwardly and the *n*-type region of the substrate upwardly to form a junction.

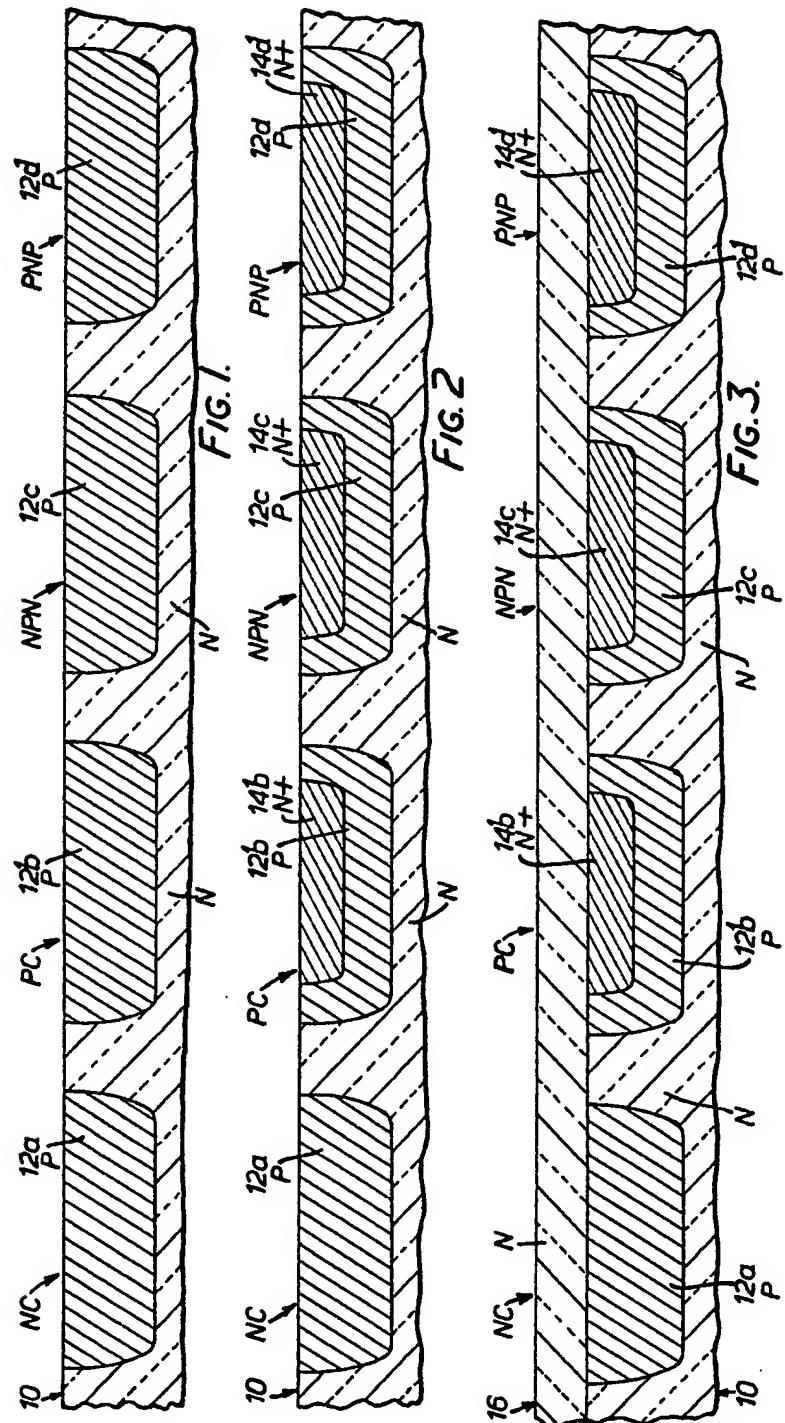
10. A semiconductor integrated circuit comprising a plurality of isolated semiconductor devices including a *p*-type channel field effect transistor formed in a monolithic chip, said field effect transistor having a 130

- p*-type region formed in a semiconductor substrate, a diffused *n*-type back gate region formed in said *p*-type region, an *n*-type epitaxial layer grown over said back gate 5 region, a *p*-channel region diffused partially through the epitaxial layer above said back gate region, said channel region extending downwardly and said back gate region extending upwardly to form a *p-n* junction 10 therebetween in said epitaxial layer, isolation rings formed about each of the semiconductor devices including the field effect transistor, and *p*-type source and drain regions and an *n*-type front gate region 15 formed in said channel region.
11. A semiconductor integrated circuit according to Claim 10, which further includes a *n*-channel field effect transistor complementary to said *p*-channel field effect 20 transistor, said *n*-channel field effect transistor comprising a *p*-type back gate region formed during the formation of the first-mentioned *p*-type region for the *p*-channel field effect transistor, said back gate region 25 being covered by said *n*-type epitaxial layer, said *p*-type back gate region being diffused upwardly to form an advance front *p-n* junction in said epitaxial layer at a depth
- substantially identical to that of the junction formed in the *p*-channel field effect transistor, a diffused front gate of *p*-type conductivity formed during diffusion of the source and drain regions of the *p*-channel field effect transistor, and *n*-type source and drain regions formed in said epitaxial layer 30 during diffusion of the front gate region of the *p*-channel field effect transistor. 35
12. A method of fabricating a semiconductor integrated circuit substantially as herein described with reference to Figures 1 to 7 of the accompanying drawings. 40
13. A semiconductor integrated circuit substantially as herein described with reference to Figure 7 or 8 of the accompanying drawings. 45
14. A semiconductor integrated circuit fabricated by a method according to any of Claims 1 to 9 and 12.

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3 SHEETS

COMPLETE SPECIFICATION

This drawing is a reproduction of
the Original on a reduced scale.

SHEET 2

